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auxiliary cells comprising charge carrier transfer zones forming third pn junctions with desaturation portions of the drain construction;

a first control structure comprising a first portion of a control electrode and configured to induce an inversion channel through the body zones in an on state; 5
a second control structure directly adjoining the desaturation portions, the second control structure comprising a second portion of the control electrode and a charged layer sandwiched between the second portion of the control electrode and the desaturation portions and containing a control charge adapted to induce an inversion layer in the desaturation portions in the on state.

12. The semiconductor switching device of claim 11, wherein the control charge is adapted to induce the inversion layer in the desaturation portions at a first gate voltage applied between the control electrode and the source zones in the on state and to induce no inversion layer in the desaturation portions at a second gate voltage applied between the control electrode and the source zones in the on state. 15

13. The semiconductor switching device of claim 11, further comprising:

a first load terminal electrically connected to the source zones, the body zones and the charge carrier transfer zones, and 25
a second load terminal electrically connected to the drain construction.

14. The semiconductor switching device of claim 11, wherein the source zones, the body zones and the charge carrier transfer zones are formed in semiconductor mesas formed from portions of a semiconductor body, and the control structures separate neighboring ones of the semiconductor mesas. 30

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15. The semiconductor switching device of claim 11, further comprising:

a first dielectric sandwiched between the semiconductor body and the charged layer, and a second dielectric sandwiched between the charged layer and the control electrode.

16. The semiconductor switching device of claim 11, wherein the charged layer is a conductive layer.

17. The semiconductor switching device of claim 16, further comprising:

a wiring structure connecting the charged layer with a programming pad.

18. The semiconductor switching device of claim 11, wherein the charged layer is a dielectric charge trapping layer. 15

19. The semiconductor switching device of claim 11, wherein the first dielectrics are thicker than the second dielectrics.

20. The semiconductor switching device of claim 11, wherein the drain construction includes barrier zones and a drift zone, a mean net dopant concentration of the barrier zones exceeds at least five times a mean net dopant concentration in the drift zone and the charge storage structure is sandwiched between the control electrode and at least some of the barrier zones. 25

21. The semiconductor switching device of claim 11, wherein the charged layer is a dielectric structure embedding semiconducting nanocrystallites.

22. The semiconductor switching device of claim 11, wherein the auxiliary cells are devoid of doped zones that are both electrically connected to the first load terminal and form pn junctions with the charge carrier transfer zones. 30

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